# An Analysis of Dynamic Element Matching Digital to Analog Converters

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Abstract-Although many dynamic element matching (DEM) digital to analog converters (DACs) have identical architectures, analyses of DEM DACs have been specific to the DAC's DEM technique. In this paper, a particular DEM DAC architecture is analyzed and criteria are developed for comparing this architecture's performance when various DEM techniques are applied to it.

## I. INTRODUCTION

Dynamic element matching (DEM) is a dynamic process that can reduce the effects of component mismatches in electronic circuits. DEM techniques dynamically rearrange the interconnections of mismatched components so that the time averages of the equivalent components at each of the component positions are nearly equal. If this dynamic rearrangement is deterministic, the DEM technique is said to be deterministic, and if the dynamic rearrangement of mismatched components is stochastic, the DEM technique is said to be stochastic.

Deterministic and stochastic DEM techniques have been used to reduce the effects of component mismatches in digital to analog converters (DACs) thereby improving their performance [1; 2; 3; 4; 5; 6]. Because DEM techniques dynamically rearrange components, deterministic DEM DACs can be classified as time varying systems, and stochastic DEM DACs can be classified as random systems. Also, because DACs contain mismatched components, DACs are nonlinear



systems which implies that deterministic and stochastic DEM DACs can be classified as nonlinear time varying systems

and nonlinear random systems, respectively. As a result, analyses of DEM DACs have been specific to the DAC's DEM technique even though many DEM DACs have identical architectures. In this paper, a particular DEM DAC architecture is analyzed and criteria are developed for comparing this architecture's performance when various DEM techniques are applied to it.

# II. A DEM FLASH DAC ARCHITECTURE

Fig. 1 shows the block diagram of a *B* bit flash DAC that performs DEM by mapping a *B* bit binary input signal, x(n), where  $x_0 \le x(n) \le x_0 + 2^B - 1$  to  $2^B$  unit DACs [4]. In Fig. 1, the natural binary converter transforms the input signal, x(n), where  $x_0 \le x(n) \le x_0 + 2^B - 1$  into the *B* bit natural binary signal,  $\chi(n)$ , where  $\chi(n) = x(n) - x_0$  which implies that  $0 \le \chi(n) \le 2^B - 1$ . The modified thermometer coder converts the natural binary coded signal,  $\chi(n)$ , into a  $2^B$  bit modified thermometer coded signal, t(n). The interconnection network connects the  $2^B$  bits of the modified thermometer coded signal, t(n), to the  $2^B$  unit DACs. Regardless of the interconnection network's control signal, c(n), the interconnection network's output, g(n), activates  $\chi(n)$ , or  $x(n)-x_0$ , unit DACs and deactivates the remaining  $2^B - \chi(n)$ , or  $2^B - x(n) + x_0$ , unit DACs. If each activated unit DAC generates an analog signal, *a*, and each deactivated unit DAC generates an analog signal, *d*, the DAC's quantization step sizes or code widths, *q*, are the difference between *a* and *d*, that is q = a - d which is a constant. The DAC's output, y(nT), is the sum of all of the unit DAC outputs, that is,

$$y(nT) = a\chi(n) + \left[d2^B - \chi(n)\right]$$
$$= (a-d)\chi(n) + d2^B = \left[d\chi(n) - \chi_0\right] + \left[d^B\right].$$
(1)

In practice, mismatched components between each of the unit DACs prevent the analog outputs of the unit DACs from having identical activated and deactivated values, respectively. As a result, the DAC's quantization step sizes or code widths are not constant, the DAC's transfer characteristic is nonlinear, and the DAC's performance is degraded [7]. To improve the DAC's performance, the DEM DAC's interconnection network dynamically alters the mapping between the input signal, x(n), and the mismatched unit DACs so that the time averages of the activated and deactivated unit DAC outputs are nearly equal, respectively.

In this paper, a general analysis of the DEM DAC in

Fig. 1 is developed. Using this analysis, the DAC's mean integral nonlinearity (INL), the variance of the DAC's INL, the DAC's output signal to distortion ratio (SDR), and the DAC's output signal to noise plus distortion ratio (SNDR) can be calculated and used as criteria to compare DEM DACs using various interconnection networks and control signals.

### **III. AN ANALYSIS OF DEM DACS**

In Fig. 1, the DEM DAC's output, y(nT), is a function of t(n) which is a function of x(n), the interconnection network, the interconnection network's control signal, c(n), and the activated and deactivated analog outputs generated by each of the unit DACs.

To express t(n) as a function of x(n), let  $\chi_k(n)$  represent  $\chi(n)$ 's *k*th bit where  $\chi_1(n)$  is  $\chi(n)$ 's least significant bit (LSB). If t(n) is represented by the vector,  $\mathbf{T}(n)$ , where

$$\mathbf{T}(n) = \left[t_1(n), t_2(n), t_3(n), \cdots, t_{2^B}(n)\right]^T$$

the superscript T denotes transpose, and  $t_1(n)$  is t(n)'s LSB, then  $\mathbf{T}(n)$  is defined such that  $t_1(n) = 0$  and  $t_{2^{k-1}+1}(n) = \dots = t_{2^k}(n) = \chi_k(n)$ . Using the vector, **T**(*n*), to represent t(n), t(n) and x(n) can be related by

$$\mathbf{T}^{T}(n)\mathbf{T}(n) = \boldsymbol{\chi}(n) = \boldsymbol{\chi}(n) - \boldsymbol{\chi}_{0}$$

To express the interconnection network's  $2^B$  bit output signal, g(n), as a function of x(n), let the vector,  $\mathbf{G}(n)$ , represent g(n) where

$$\mathbf{G}(n) = \left[g_1(n), g_2(n), \cdots, g_{2^B}(n)\right]^T$$

and  $g_1(n)$  is g(n)'s LSB. Because G(n) is a function of c(n)and t(n), which is a function of x(n), the interconnection network can be represented by the transformation  $\mathcal{T}_{\mathbf{G}}$  such that

$$\mathbf{G}(n) = \mathcal{T}_{\mathbf{G}}[x(n), c(n)]. \tag{2}$$

Regardless of the transformation  $\mathcal{T}'_{\mathbf{G}}$  and c(n),

$$\mathbf{G}^{T}(n)\mathbf{G}(n) = \mathbf{T}^{T}(n)\mathbf{T}(n) = \boldsymbol{\chi}(n) = \boldsymbol{x}(n) - \boldsymbol{x}_{0}, \qquad (3)$$

and thus, the interconnection network activates  $\chi(n)$ , or x(n)- $x_0$ , unit DACs and deactivates the remaining  $2^B - \chi(n)$ , or  $2^B$  $x(n)+x_0$ , unit DACs.

To express y(nT) as a function of G(n), define the output,  $y_k(nT)$ , of the kth unit DAC as

$$y_k(nT) = \begin{cases} a_k, & g_k(n) = 1 \\ d_k, & g_k(n) = 0 \end{cases} = \begin{cases} \overline{a} + h_k, & g_k(n) = 1 \\ \overline{d} + l_k, & g_k(n) = 0 \end{cases}$$

where  $a_k$  and  $d_k$  are the values of the activated and deactivated kth unit DAC, respectively,

$$\overline{a} = \frac{1}{2^{B}} \sum_{k=1}^{2^{B}} a_{k},$$
  
$$\overline{d} = \frac{1}{2^{B}} \sum_{k=1}^{2^{B}} d_{k}.$$
 (4)

 $h_k = a_k - \overline{a}$ , and  $l_k = d_k - \overline{d}$ . As a result, the DAC's output, v(nT), can be written as

$$y(nT) = \sum_{k=1}^{2^{B}} y_{k}(nT)$$
$$= \overline{a} \mathbf{G}^{T}(n) \mathbf{G}(n) + \mathbf{G}^{T}(n) \mathbf{H}$$
$$+ \overline{d} [\mathbf{1} - \mathbf{G}(n)]^{T} [\mathbf{1} - \mathbf{G}(n)] + [\mathbf{1} - \mathbf{G}(n)]^{T} [\mathbf{1} - \mathbf{G}(n)] + [\mathbf{1} - \mathbf{G}(n)]^{T} [\mathbf{1}$$

 $+ \overline{d} [\mathbf{1} - \mathbf{G}(n)]^T [\mathbf{1} - \mathbf{G}(n)] + [\mathbf{1} - \mathbf{G}(n)]^T \mathbf{L} \quad (5)$ where  $\mathbf{H} = [h_1 \cdots h_{2^B}]^T$ ,  $\mathbf{L} = [l_1 \cdots l_{2^B}]^T$  and  $\mathbf{1}$  is a  $2^{B}$  x 1 vector of ones. <sup>2</sup>Substituting (3) into<sup>2</sup>(5) and defining  $\overline{q}$  as the DAC's average code width, which implies that  $\overline{q} = (\overline{a} - \overline{d})$ , the DAC's output, y(nT), can be written as  $y(nT) = (\overline{a} - \overline{d})[x(n) - x_0] + \overline{d}2^B$ 

$$+ \mathbf{G}^{T}(n)\mathbf{H} + [\mathbf{1} - \mathbf{G}(n)]^{T}\mathbf{L}$$
$$= \overline{q}[x(n) - x_{0}] + \overline{d}2^{B} + \mathbf{G}^{T}(n)(\mathbf{H} - \mathbf{L}) + \mathbf{1}^{T}\mathbf{L} \qquad (6)$$

Because  $d_k = \overline{d} + l_k$ , (4) can be written as

$$\overline{d} = \frac{1}{2^B} \sum_{k=1}^{2^B} \overline{d} + l_k \,,$$

which implies that

$$\sum_{k=1}^{2^B} l_k = \mathbf{1}^T \mathbf{L} = 0.$$
 (7)

Similarly, because  $a_k = \overline{a} + h_k$ ,

$$\sum_{k=1}^{2^B} h_k = \mathbf{1}^T \mathbf{H} = 0.$$
(8)

Substituting (2) and (7) into (6), the DAC's output can be written as

$$y(nT) = \overline{q}[x(n) - x_0] + \overline{d}2^B + \mathcal{T}_{\mathbf{G}}^T[x(n), c(n)](\mathbf{H} - \mathbf{L}).$$
(9)  
In (9) the term  $\overline{a}[x(n) - x_0] + \overline{d}2^B$  is similar to the ideal

In (9), the term,  $\overline{q} |x(n) - x_0| + d2^{D}$ , is similar to the ideal DAC's output in (1), and represents the DAC's output when all of the unit DAC's activated and deactivated analog outputs are identically  $\overline{a}$  and d, respectively. Therefore, the last term,  $\mathcal{T}_{\mathbf{G}}^{T}[x(n), c(n)](\mathbf{H} - \mathbf{L})$ , in (9), is the DAC's nonlinear transformation that describes the DAC's INL.

When calculating performance criteria for the DEM DAC in Fig. 1, it is necessary for the DC power in the DAC's digital input, x(n), and the DC power of DAC's undistorted output,  $\bar{q}[x(n) - x_0] + \bar{d}2^B$ , to be equal. Therefore, this paper assumes that  $x_0 = \bar{d}2^B / \bar{q}$  which implies that

 $y(nT) = \mathcal{T}[x(n), c(n)] = \overline{q}x(n) + \mathcal{T}_{INL}[x(n), c(n)].$ (10) where  $\mathcal{T}$  represents the DAC's transformation and  $\mathcal{T}_{INL}$ represents the transformation of the DAC's INL, that is,

$$\mathcal{T}_{INL}[x(n), c(n)] = \mathcal{T}_{\mathbf{G}}^{T}[x(n), c(n)](\mathbf{H} - \mathbf{L}).$$

## IV. PERFORMANCE CRITERIA FOR DEM DACS

In this section, the mean of the DAC's INL, the variance of the DAC's INL, the DAC's SDR, and the DAC's SNDR are determined for stochastic DEM DAC. These performance criteria can also be applied to deterministic DEM DACs by replacing the probabilistic means and variances with arithmetic means and variances, respectively.

To calculate the mean of a stochastic DEM DAC's INL, apply the expectation operator conditioned on the input signal, x(n), to the DAC's output in (10) that is,

$$E[y(nT)|x(n)] = \overline{q}x(n) + E\left\{\mathcal{T}_{\mathbf{G}}^{T}[x(n), c(n)]|x(n)\right\}(\mathbf{H} - \mathbf{L}).$$
(11)

In (11), the term,  $\bar{q}x(n)$ , represents the DAC's output when all of the DAC's code widths are identically  $\bar{q}$ , and therefore, the second term,  $E\{\mathcal{T}_{\mathbf{G}}^{T}[x(n), c(n)] | x(n)\}(\mathbf{H}-\mathbf{L})$ , in (11) is the stochastic DEM DAC's expected INL for a particular input, x(n), that is,

$$E\left[\mathcal{T}'_{INL} \middle| x(n)\right] = E\left\{\mathcal{T}'_{\mathbf{G}}^{T}[x(n), c(n)] \middle| x(n)\right\} (\mathbf{H} - \mathbf{L}).$$
(12)

Using (12), a stochastic DEM DAC's INL variance,  $\sigma_{\mathcal{T}_{INL}|x}^2$ , conditioned on x(n) can be calculated as

$$\sigma_{\mathcal{T}_{INL}|x}^{2} = (\mathbf{H} - \mathbf{L})^{T} \left[ E \left\{ \mathcal{T}_{\mathbf{G}}^{'} \mathcal{T}_{\mathbf{G}}^{'T} \middle| x(n) \right\} - E \left\{ \mathcal{T}_{\mathbf{G}}^{'} \middle| x(n) \right\} E \left\{ \mathcal{T}_{\mathbf{G}}^{'T} \middle| x(n) \right\} \right] (\mathbf{H} - \mathbf{L}) .$$
(13)

which is also the DAC's output variance,  $\sigma_{y|x}^2(n)$ , conditioned on x(n), that is,

$$\sigma_{y|x}^2 = \sigma_{T'_{INL}|x}^2.$$
(14)

Two other criteria used to measure a DAC's performance are SDR and SNDR. To calculate a stochastic DEM DAC's SDR, assume that the DAC's analog output, y(t), is an impulse train weighted by y(nT), that is,

$$y(t) = \sum_{n=-\infty}^{\infty} y(nT)\delta(t-nT)$$

where  $\delta(t)$  is the Dirac delta function. Using this assumption, the DAC's average signal plus distortion power,  $P_y$ , can be written as

$$P_{y} = E\left[y^{2}(nT)\right] = E\left\{E\left[y^{2}(nT)|x(n)\right]\right\}.$$
 (15)

Substituting (10) into (15),  $P_y = P_{y_l} + P_{y_e}$ 

 $P_{y_l} = \overline{q}^2 E \left[ x^2(n) \right]$ 

and

$$P_{y_e} = 2 \overline{q} E \bigg\{ x(n) E \bigg[ \mathcal{T}_{INL} \bigg| x(n) \bigg] \bigg\} + \sigma_{\mathcal{T}_{INL}}^2 + E^2 \bigg[ \mathcal{T}_{INL} \bigg].$$

In (16), the first term,  $P_{yl}$ , is the average output power of a linear DAC with code widths  $\bar{q}$  and the second term,  $P_{ye}$ , is the average power of the output's conversion errors or distortion. Therefore, the DAC's SDR is

$$SDR = \frac{\overline{q}^2 E[x^2(n)]}{2\overline{q} E\left\{x(n) E[\mathcal{T}_{INL} | x(n)]\right\} + \sigma_{\mathcal{T}_{INL}}^2 + E^2[\mathcal{T}_{INL}]}.$$
 (17)

To calculate a stochastic DEM DAC's SNDR, consider an input, x(n), which can be written as

$$x(n) = s(n) + w(n)$$

X

where s(n) is the signal component of the DAC's input and w(n) is an independent zero mean white noise component of the DAC's input. Using (10), the DAC's output, y(nT), can be written as

$$y(nT) = \mathcal{T}[s(n) + w(n), c(n)]$$
  
=  $\overline{a}s(n) + \overline{a}w(n) + \mathcal{T}_{DM}[s(n) + w(n), c(n)]$  (18)

$$= q_{s}(n) + q_{w}(n) + 1_{INL}[s(n) + w(n), c(n)].$$
(18)  
Substituting (18) into (15),  
$$P_{y} = P_{y_{l}} + P_{y_{n+d}}$$
(19)

where

$$P_{y_l} = \overline{q}^2 E[s^2(n)]$$

and

$$\begin{split} P_{y_{n+d}} &= \overline{q}^2 E \Big[ w^2(n) \Big] + \sigma_{\mathcal{T}_{INL}}^2 + E^2 \Big[ \mathcal{T}_{INL} \Big] \\ &+ 2 \overline{q} E \Big\{ x(n) E \Big[ \mathcal{T}_{INL} \Big| x(n) \Big] \end{split}$$

where x(n) = s(n) + w(n). In (19), the first term,  $P_{yl}$ , is the average output power of a linear DAC with code widths  $\bar{q}$  and the second term,  $P_{y_n+d}$ , is the average power of the output's noise plus distortion. Therefore the DAC's SNDR is

$$SNDR = \frac{\overline{q}^{2} E[s^{2}(n)]}{\left(\overline{q}^{2} E[w^{2}(n)] + \sigma_{\mathcal{T}_{INL}}^{2} + E^{2}[\mathcal{T}_{INL}]\right)} + 2\overline{q} E\left\{x(n) E[\mathcal{T}_{INL}|x(n)]\right\}}.$$
(20)

To calculate the mean of the INL, the variance of the INL, the SDR, and the SNDR for a deterministic DEM DAC, replace the probabilistic means and variances in (12), (14), (17) and (20) with arithmetic averages and variances, respectively.

#### IV. STOCHASTIC DEM DACS

For stochastic DEM DACs, interconnection networks are often chosen and controlled such that

$$E[y(nT)|x(n)] = \overline{q}x(n).$$
(21)

which implies that

(16)

$$E\left[\mathcal{T}_{INL}^{T}\middle|x(n)\right] = E\left\{\mathcal{T}_{\mathbf{G}}^{T}\left[x(n), c(n)\right]\middle|x(n)\right\} (\mathbf{H} - \mathbf{L}) = 0.$$
(22)

For these types of stochastic DEM DACs, the performance criteria described by (14), (17) and (20) can be simplified by substituting (22) into these equations. Substituting (22) into (14),

$$\sigma_{\mathcal{T}_{INL}|x}^{2} = (\mathbf{H} - \mathbf{L})^{T} E \Big[ \mathcal{T}_{\mathbf{G}} [x(n), c(n)] \\ \times \mathcal{T}_{\mathbf{G}}^{T} [x(n), c(n)] |x(n)] (\mathbf{H} - \mathbf{L}).$$
(23)

which is also the DAC's mean squared INL for a particular x(n). Substituting (22) into (17), the DAC's SDR is

$$SDR = \frac{P_{y_a}}{P_{y_e}} = \frac{\overline{q}^2 E[x^2(n)]}{\sigma_{T'_{INL}}^2},$$
(24)

and substituting (22) into (20), the DAC's SNDR becomes

$$SNDR = \frac{\overline{q}^2 E[s^2(n)]}{\overline{q}^2 E[w^2(n)] + \sigma_{\mathcal{T}_{INL}}^2}.$$
 (25)

## IV. EXAMPLE

Consider a six bit linear DAC that has a full scale dithered sinusoidal input with a frequency of  $313\pi/2048$  radians/sample. The dither sequence is a strictly white sequence with a triangular probability distribution function supported on (-q,q). Fig. 2(a) shows the power spectral density (PSD) of the simulated DAC's output. The PSD was obtained by averaging 40 periodograms each corresponding to  $2^{12}$  samples of the dithered sinusoid input sequence. For this example, consider the DEM DAC in Fig. 1 where the unit DACs have linear gradient errors that vary linearly from +5% to -5% of an LSB and uniformly distributed random errors that are uniformly distributed between +2% and -2% of an LSB. Fig. 2(b) shows the PSD of the nonlinear DAC's output. This PSD was also obtained by averaging 40 periodograms each corresponding to  $2^{12}$  samples.

For this example, the interconnection network is the Benes network in [5] where c(n) is an independent white uniformly distributed stochastic signal. Fig. 2(c) shows the PSD of this stochastic DEM DAC's output. For this network and control signal, it can be shown [5] that

$$E\left[\mathcal{T}_{\mathbf{G}} \middle| x(n)\right] = \frac{\chi(n)}{2^{B}} \mathbf{1},$$

which implies  $E[\mathcal{T}'_{INL}|x(n)] = 0$ , and thus the DAC's average transformation can be described by (21). It can also be shown [5] that

$$E\left[\mathcal{T}_{\mathbf{G}}^{'}\mathcal{T}_{\mathbf{G}}^{'T}|x(n)\right] = \frac{\chi(n)[\chi(n)-1]}{2^{B}(2^{B}-1)}\mathbf{1}_{2^{B}} + \frac{\chi(n)[2^{B}-\chi(n)]}{2^{B}(2^{B}-1)}\mathbf{I}_{2^{B}}$$

where  $\mathbf{I}_{2^B}$  is the  $2^B$  by  $2^B$  identity matrix and  $\mathbf{1}_{2^B}$  is the  $2^B$  by  $2^B$  ones matrix. Using (24), the DAC's SDR is 41.9 dB, and using  $40 \times 2^{12}$  samples, the DAC's experimental SDR is 41.9 dB. Assuming the DAC's input, x(n), has the form, s(n)+w(n), where s(n) is the unquantized sinusoidal input without dither and w(n) is the signal that includes quantization and dither noise, the DAC's SNDR is 31.5 dB using (25). Using  $40 \times 2^{12}$  samples, the DAC's experimental SNDR is 31.5 dB.

#### V. SUMMARY

In this paper, the DEM DAC architecture in Fig. 1 is analyzed and described by the transformation in (10). Using (10), expressions for the DAC's mean INL, the variance of the DAC's INL, the DAC's SDR, and the DAC's SNDR were developed and are described by (12), (13), (17) and (20), respectively. The expressions in (13), (17) and (20) were further simplified in (23), (24) and (25) for DAC's that have zero mean INL. Using these criteria, a stochastic DEM DAC that uses a Benes interconnection network is analyzed, and theoretical results are compared to experimental simulated results.



Fig. 2. Power spectral density for (a) linear six bit DAC, (b) nonlinear six bit DAC and (c) stochastic Benes network DEM DAC.

#### REFERENCES

- R.J. Van de Plaasche, "Dynamic element matching for high accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 795-800, Dec. 1976.
- [2] B.H. Leung and S. Sutrarja, "Multibit ΔΣADC incorporating a novel class of dynamic element matching techniques," *IEEE Trans. Circuits* and Systems II: Analog and Digital Signal Proc., vol. 39, no. 1, pp. 35-51, Jan. 1992.
- [3] R.T. Baird and T.S. Fiez, "Linearity enhancement of multibit  $\Delta\Sigma$  A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits and Systems II: Analog and Digital Signal Proc.*, vol. 42, no. 12, pp. 753-762, Dec. 1995.
- [4] L.R. Carley, "A noise shaping coder topology for 15+ bits converters," IEEE J. Solid-State Circuits, vol. SC-24, pp. 267-273, 1989.
- [5] I. Galton, P. Carbone, "A rigorous error analysis of D/A conversion with dynamic element matching," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 763-772, 1995.
- [6] J.W. Bruce and P. Stubberud, "Generalized cube networks for implementing dynamic element matching digital-to-analog converters," *Proc. of the Midwest Symposium on Circuits and Systems*, pp. 522-525, Aug. 1998.
- [7] P. Stubberud and J.W. Bruce, "An analysis of harmonic distortion and integral nonlinearity in digital to analog converters," *Proc. of the Midwest Symposium on Circuits and Systems*, August 1999.